Customer No.: 31561
Application No.: 10/604,587
Docket No.: 10264-US-PA-1

REMARKS

Present Status of the Application

Applicants would like to think Examiner for the careful review of this application. The Office Action rejected claims 1-9 under 35 U.S.C. 103(a) as being unpatentable over Chang (US 6,541,828) (hereinafter Chang) in view of Ko (US 6,479,864) (hereinafer Ko) and Li et al. (US 6,545,310). Claims 1, 2, 8 and 9 have been amended to more appropriately define the invention. New claims 15-24 have been added. The amendment is fully supported by the original application field on July 31, 2003. No new matter has been added. Upon entry of the amendment, Claims 1-9 and 15-24 are pending.

DISCUSSION OF OFFICE ACTION REJECTIONS

Response To 35 U.S.C. 103 (a) Rejection

Claims 1 to 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US 6,541,828) in view of Ko (US 6,479,864) and Li et al (US 6,545,310).

Applicant traverses the rejection of claims 1-9 under *35 U.S.C. 103(a)* as being unpatentable over Chang in view of Ko and Li because a *prima facie* case of obviousness has not been established by the Examiner.

To establish a *prima facie* case of obviousness under *35 U.S.C. 103(a),* each of three requirements must be met. First, the reference or references taken alone or combined must teach or suggest each and every element recited in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one skill in the art, to combine the reference in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of three requirements must "be found in the prior art, and not be based on applicant's disclosure". *See* M.P.E.P. §2143, 8th ed., February 2003.

Applicant first submit that, Chang in view of Ko and Li. is legally deficient for the purpose of rendering claims 1 to 9 unpatentable for at least the reason that not every element of the claim was taught or suggested by cited references such that the invention as a whole would have been obvious to one of ordinary skill in the art.

The present invention is in general related to a method of fabricating a non-volatile memory. Particularly, claim 1 recites "forming a longitudinal strip of stacked layer over the substrate, wherein the longitudinal strip is a stack that includes a gate dielectric layer, a conductive layer and a cap layer; patterning the longitudinal strip to form a plurality of stacked blocks; forming a dielectric layer over the substrate, wherein the dielectric layer exposes the cap layers of the stacked blocks; removing the cap layers of some of the stacked blocks to form a plurality of first opening exposing a portion of the conductive layer of the stacked blocks; and forming a word line over the dielectric layer and filling the first openings to connect the portion

of the conductive layer exposed by the first opening of the stacked blocks in the same row serially to form a plurality of coding memory cells, wherein the coding memory cells having the word line connecting to the conductive layer of the stacked blocks are in a first data state and the coding memory cells having the word line connecting to the cap layers of the stacked blocks are in a second data state."

Chang discloses a method of fabricating a non-volatile ROM. The method is applied for forming a dielectric layer over the word lines and gate oxide layer and for performing an ion implanting a code implant dopant into the substrate. *See* ABSTRACT.

In the Office Action, the Examiner seemed to consider Chang's dielectric layer 48 as corresponding to Applicant's claimed dielectric layer.

Applicants point out that, according to Chang, "the polysilicon layer (word line) 44 and the gate oxide layer 42 are covered with a dielectric layer 48". See col. 3 lines 49-50, and Fig. 5A. Apparently, the dielectric layer 48 is formed over the word line 44. Therefore, Chang fails to teach "forming a word line over the dielectric layer", as recited in claim 1. In addition, Chang also fails to teach "forming a longitudinal strip of stacked layer over the substrate, wherein the longitudinal strip is a stack that includes a gate dielectric layer, a conductive layer and a cap layer; patterning the longitudinal strip to form a plurality of stacked blocks; forming a dielectric layer over the substrate, wherein the dielectric layer exposes the cap layers of the stacked blocks; removing the cap layers of some of the stacked blocks to form a plurality of first opening exposing a portion of the conductive layer of the stacked blocks; and forming a word line over

the dielectric layer and filling the first openings to connect the portion of the conductive layer exposed by the first opening of the stacked blocks in the same row serially to form a plurality of coding memory cells, wherein the coding memory cells having the word line connecting to the conductive layer are in a first data state and the coding memory cells having the word line connecting to the cap layers are in a second data state".

In the Office Action, the Examiner asserted that Chang and Ko are both the same field of endeavor, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Chang by the longitudinal strip having a cap layer, a conductive layer and gate dielectric layer as taught by Ko to preventing layer not aligned with the selected pattern.

In the present invention, "the coding memory cells having the word line connecting to the conductive layer of the stacked blocks are in a first data state and the coding memory cells having the word line connecting to the cap layer of the stacked blocks are in a second data state" is taught in claim 1. In other words, the mask ROM coding method according to this invention utilizes the connectivity between the word line and the conductive layer of the stacked block instead of a conventional cod implant process to code the memory device. The fact that Cheng requires that performing an ion implanting a code implant dopant into the substrate would render it unreasonable to further forming a stacked blocks for coding. Thus, Cheng, in fact teaches away from the recitation of claim 1. Moreover, the formation of the stacked block formed on the channel region is adverse for performing the ion implantation of coding process because of longer distance. Therefore, one skilled in the art would not be motivated or suggested to apply

Ko's teachings in practicing Cheng. Nor would there be any reasonable expectation of success in doing so, in view of such a teaching away reference.

Furthermore, Ko discloses a semiconductor structure including gate stacks having a polysilicon layer 24, a refactory metal silicon layer 26, and an undoped silicon dioxide layer 30. Applicant submit that Ko does not teach or suggest "removing the cap layers of some of the stacked blocks to form a plurality of first opening exposing a portion of the conductive layer of the stacked blocks; and forming a word line over the dielectric layer and filling the first openings to connect the portion of the conductive layer of the exposed by the first opening of the stacked blocks.....".

On the other hand, Li discloses a non-volatile memory. Each word line of the memory is connected to the control gate. *See* Fig. 3. Applicant submit that Li does not teach or suggest "the coding memory cells having the word line connecting to the conductive layer of the stacked blocks are in a first data state and the coding memory cells having the word line connecting to the cap layer of the stacked blocks are in a second data state" as taught in claim 1.

Therefore, Ko and Li et al. do not cure the deficiencies of Cheng.

Thus, claim 1 is patentable over over Chang in view of Ko and Li. Claims 2-9 are also patentable over Chang in view of Ko and Li at least because of their dependency from an allowable base claim.

In making the rejections of claim 2, the Examiner alleged that "Ko further discloses tha cap layer 48 having a greater etch rate than the dielectric layer 22". Applicant point that,

according to Ko, "Undoped silicon dioxide layer 48 on each gate stacks 50 of second series 74 acts as an etch mask, thereby preventing the etchant system from removing material from doped silicon dioxide layer 22 except as aligned with first selected pattern 66". *See* col. 7, lines 64-67. In order to act as an etch mask, the Undoped silicon dioxide layer 48 must have a lower etch rate than the dielectric layer 22. Thus, Ko. in fact teaches away from the recitation of claim 2. Ko and Li et al. do not cure the deficiencies of Cheng.

In view of the foregoing remarks, Applicant respectfully requests that the rejection under § 103(a) be withdrawn and that claims 1-9 be allowed.

New added claims

New added claims 15-24 are patently define over the prior art references in view of the aforementioned remarks, and should be allowed.

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CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-9 and 15-24 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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